Abstract of the Disclosure

A delay cell has selectable numbers of parallel load resistance transistors operable in parallel, and a similarly selectable number of bias current transistors connectable in parallel. The delay cell is preferably differential in construction and operation. A voltage controlled oscillator ("VCO") includes a plurality of such delay cells connected in a closed loop series. Phase locked loop ("PLL") circuitry includes such a VCO controlled by phase/ frequency detector circuitry. The PLL can have a very wide range of operating frequencies as a result of the ability to control the number of load resistance transistors and bias current transistors that are active or inactive in each delay cell. Such activation/deactivation may be programmable or otherwise controlled.